•Slides 1-13:
Industry Buzz

•Slides 14-56:
Characterizing Jitter eSeminar

THE 40G INDUSTRY BUZZ

February 5, 2002

presented by:

Larry DesJardin

Agilent Technologies

THE 40G Industry Buzz

- Industry Update & Commentary
- "Late Breaking News" from Agilent
- Viewer Poll & Feedback

THE 40G Industry Buzz

- ***Industry Update & Commentary***
- **"Late Breaking News" from Agilent**
- **Viewer Poll & Feedback**

40G Interconnects

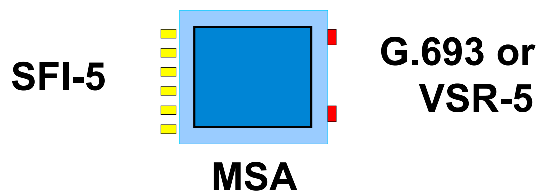
- 40G interfaces will be used for very short reach and long reach applications
- Long reach will typically be DWDM-based
- Short Reach and Very Short Reach (VSR) will typically be used to interconnect equipment within the same building or neighborhood.
- VSR will typically be a single wavelength over a single fiber, or parallel fibers, not DWDM

40G Transponders

- VSR Interfaces, being between different vendors, require standards.
- This standardization allows “industry standard transponders” to be created
- Standardized transponders require:
  - Standardized Electrical Interface specs
  - Standardized Optical Interface specs
  - Standardized Packaging and Pinout

40G Transponder Standards

- Electrical Interface = SFI-5
- VSR Serial Interface = G.693
- VSR Parallel Interface = OIF VSR-5
- Pinout and Packaging will be “MSAs”



40G Transponder Standards: MSAs

- MSA= Multi-Source Agreement
- Typically a private agreement
- First MSA announced, includes Agere Systems, Agilent Technologies, Alcatel Optronics, Ericsson Microelectronics, ExceLight, JDS Uniphase, Mitsubishi, NEC, and OpNext.

THE 40G Industry Buzz

- Industry Update & Commentary
- *"Late Breaking News" from Agilent*
- Viewer Poll & Feedback

Late Breaking Agilent News

The ever-increasing demand for transmission bandwidth drives the need for test of both loss and dispersion of optical components.

- Agilent 81910A
  - Designed for All Parameter Test
  - Simultaneous measurement of Loss, PDL, GD and DGD in a single connection setup
  - Accurate, hi-throughput measurement of optical components
  - Evolution of the industry standard for loss measurements
  - Integrated optical bench

Late Breaking Agilent News

New Optical Test Products:

- Agilent 8157xA Optical Attenuators
  - Up to 1 Watt for Raman
  - Flat over wavelength
  - Power control integrated

- Agilent 8159x Optical Switches
  - 1x2, dual 1x2, 2x2, 1x4
  - Automated signal routing
  - Repeatability +/- 0.005 dB

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THE 40G Industry Buzz

- Industry Update & Commentary
- “Late Breaking News” from Agilent
- *Viewer Poll & Feedback*

Viewer Poll and Feedback

Will 40Gb/s first be used for

a) Short Reach Interfaces

b) Long Haul transport

c) Too close to call.......

- **Send responses to larry_desjardin@agilent.com**
- **Individual responses remain confidential, only summary of results displayed.**
- **Results to be shown next month!**

THE 40G
INDUSTRY BUZZ

Send any feedback to:

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Characterizing Jitter On High-Speed Communications Signals

February 5, 2001

presented by:

Brian Scott

Agenda

- A review of jitter fundamentals
  - What it is and how it is generated
  - The effect of jitter on communications systems
- SONET/SDH and Ethernet timing architectures
- Characterizing jitter performance using the SONET/SDH approach
  - on transmitters
  - on receivers
- Characterizing jitter performance the Ethernet approach on receivers
  - on transmitters
  - on receivers
- Jitter measurement solutions

In today's discussion there will be some review of the basics of jitter and some of the key timing architectures before jumping into the main topic of discussion: making measurements

Jitter fundamentals: What is jitter?

- *"Deviation of the significant instants of a signal from their ideal positions in time"*
  - What is a significant instant?
  - What is the ideal position in time?

The typical one sentence description of jitter is:

"Deviation of the significant instants of a signal from their ideal positions in time".

Let's deconstruct this statement to better understand it:

What is a significant instant?

What is the ideal position in time?

Jitter-free signals have constant bit periods

- ***Significant instants*** **can usually be defined as edges**
- **The system clock can be used to define what the *ideal positions* in time are**
- **Edge position of the data should consistently align with the same relative points on the reference clock waveform**

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By examining the edges of a digital communications bit stream, we can better illustrate our definition.

Here is an oscilloscope display of a data stream with the system clock waveform, the lower display being a closeup view of the edges.

If the timing of this bit stream were jitter free, the period for all of the bits would always be precisely identical.

Thus the time between any two rising or two falling edges will always be a precise integer multiple of the nominal bit period.

Another way to look at this is to look at the data stream relative to an ideal clock source.

The time between a data edge and the closest clock edge should always be the same.

If the data signal is jitter free, then the 50% amplitude points on the data waveform should consistently align with points on the clock waveform.

However, if the bit period fluctuates for any reason, the bit stream will no longer be jitter free.

What does jitter look like?

- For most, an intuitive display is in the time domain
  - Pulse trains
  - Eye diagrams
- The signal can also be displayed in the frequency domain
  - Clock signal spectrum
  - Data signal spectrum

•To quantify jitter, it helps to display the signal in an understandable format.

•Typically, the most intuitive representation of jitter is an “amplitude versus time” format.

•This is achieved with an oscilloscope with sufficient bandwidth for the signal being analyzed.

•Depending upon how the scope is triggered, the waveform is displayed as either the pulse train (which was shown on the last slide) or the eye diagram.

•There is also value in displaying the signal as a function of frequency.

•The spectrum of a signal and it’s frequency components are displayed directly as either the clock or data signal spectrum

Jitter as seen on a pulse train

- Oscilloscope triggered with a signal that is synchronous to the pattern
- Easy to understand display of jitter
- Need to scan the entire pattern to verify the worst case bits

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•When the oscilloscope is triggered with a signal that is synchronous to the pattern

(e.g. an edge that is generated once for every repetition of the pattern),

the pulse train will be displayed.

•As discussed earlier, it is easy to get a direct view of the timing variation of data pulses.

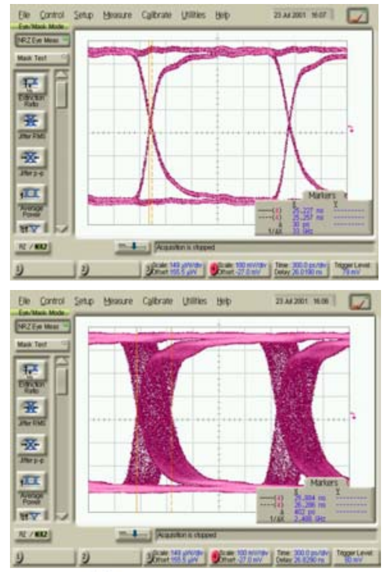
•However, the downside to displaying the signal as a pulse train, is that it is difficult to view more than a few pulses at a time.

•In most signals, the deviation of the pulses from the ideal can be impacted to a large extent by the data pattern.

•Thus, it can be difficult to determine the worst case jitter without scanning, or, sequentially “walking” through, the entire pattern

Jitter as seen on the eye-diagram

- Oscilloscope triggered with a synchronous clock
- If all bits do not have identical periods, the crossing points widen
- Crossing point width is a direct measure of the total (worst case) jitter on the signal
- 1 Unit Interval is equivalent to one bit period of jitter
  - The point at which the eye closes



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•An alternative to displaying the pulse train of the signal is to view it with an eye-diagram.

•This is a superposition of a multitude of samples throughout the entire data pattern.

•The eye diagram is achieved through triggering the oscilloscope with a synchronous clock (or divided clock).

•As the oscilloscope is in an infinite persistence mode, the eye diagram builds up and then is a good indication of the overall jitter performance.

•The width of the crossing point is a common location to quantify the jitter.

•In the lower eye diagram, the jitter is 0.25 unit intervals, where a unit interval is used to normalize the jitter to a bit period.

•One unit interval is equivalent to one bit period of jitter.

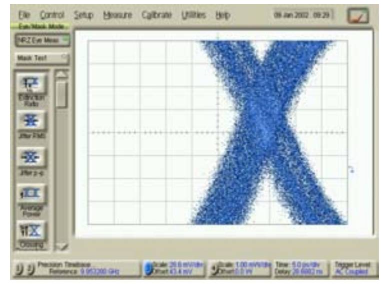
•(Note that any jitter on the trigger signal will affect the jitter measurement of the data.

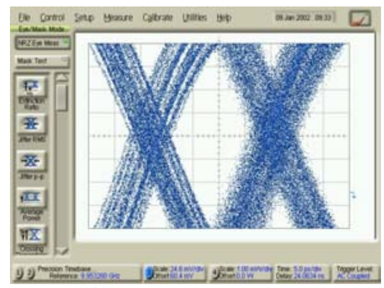
•Jitter that is common to both the data and the trigger signal can result in this jitter not being displayed on the eye diagram.

•This is most likely when the triggering clock is derived from the data itself.

Jitter as seen on eye-diagrams

- Jitter can be due to both deterministic and random phenomenon
- When the crossing point of an eye is viewed close up, the signal spread can be "smeared" by the jitter of the oscilloscope
- Using an ultra-low jitter oscilloscope, both pattern dependent and random jitter can be revealed





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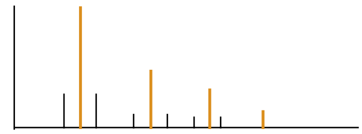
If the eye diagram is viewed on an oscilloscope that has very low intrinsic jitter, both the pattern dependent jitter , i.e., the deterministic jitter, and random jitter can be revealed, by viewing the crossing point close up.

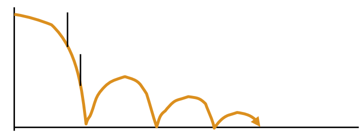
Here, the upper crossing point is viewed on an oscilloscope with typical intrinsic jitter, which results in a smeared signal spread, whereas the crossing point on the lower display is viewed with an oscilloscope with ultra-low intrinsic jitter.

Jitter in the frequency domain

- **Jitter can be considered as a form of phase modulation**
- **Difficult to intuitively gauge the magnitude of the jitter, but provides a direct indication of the *rate* of some deterministic jitter mechanisms**
- **Very good sensitivity in gauging small levels of jitter**



Clock spectrum



Data spectrum

•Because jitter can be considered as a form of phase modulation, jitter can be viewed as a function of frequency, and therefore it is very easy to see if there are any systematic elements to the jitter.

•While it is difficult to intuitively gauge the magnitude of the jitter, jitter in the frequency domain provides a direct indication of the *rate* of some deterministic jitter mechanisms

•It is also has very good sensitivity in gauging small levels of jitter

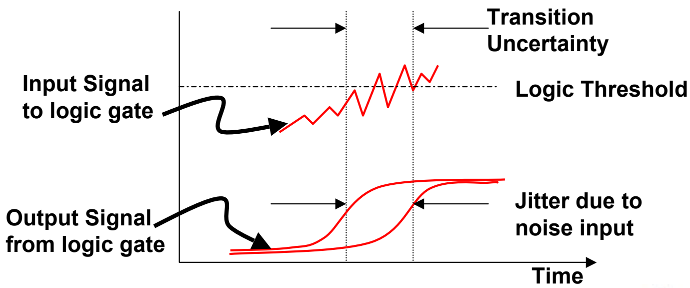
For example, if a switching power supply were causing a clock frequency to deviate from ideal, modulation sidebands would be present and easily viewed in the frequency domain plot of the clock spectrum.

Modulation sidebands can also be seen on data signals, but in general the spectrum of the data signal is complex.

Tools for examining in the frequency domain include spectrum analyzers and phase noise systems

What causes jitter?

- Jitter From Electrical Components
  - Random electrical noise resulting in intrinsic phase noise on the signal output from oscillators
  - Phase noise in logic circuits resulting in transition uncertainties



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The causes of jitter are embedded within the components of the system.

Jitter From Electrical Components

Random electrical noise resulting in intrinsic phase noise on the signal output from oscillators

Phase noise in logic circuits resulting in transition uncertainties

Random jitter mechanisms

- Thermal effects
  - Example: Varying propagation velocity
- Anything that causes oscillator phase noise
  - The timing source for data does not have a precise, constant period
  - AM-to-PM conversion of amplitude noise

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Phase Noise of Reference Clock,

Thermal effects

Example: Varying propagation velocity

Anything that causes oscillator phase noise

The timing source for data does not have a precise, constant period

AM-to-PM conversion of amplitude noise

Deterministic jitter mechanisms

- Jitter that is consistent, predictable, and bounded
  - Switching transients cause threshold voltage variation
  - Laser turn on-times sensitive to data pattern
  - Frequency response problems cause ISI (Inter-Symbol Interference)
  - Cross-Talk between transmitter and receiver
  - Eye closure due to BW limitation in the transmission channel
  - Poor Isolation
- Since this is pattern dependent jitter, all of the above happens the same way each time they occur

Switching transients cause threshold voltage variation (thus a shift in timing)

Laser turn on-times sensitive to data pattern

Frequency response problems cause ISI (Inter-Symbol Interference)

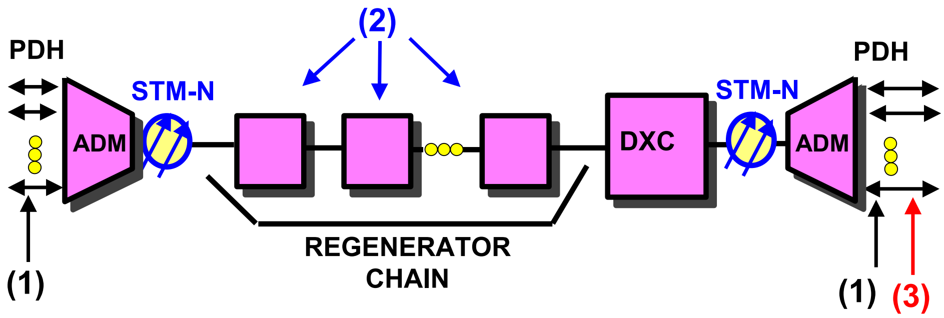
Cross-Talk between transmitter and receiver

Eye closure due to BW limitation in the transmission channel

Poor Isolation (leakage of a sinusoidal signals onto the clock, etc)

Since this is pattern dependent jitter, all of the above happens the same way each time they occur

Sources of Jitter in the SONET/SDH system



(1) Mapping Jitter, due to justification process
(2) Accumulated Jitter (Jitter Gain) due to re-timing in regenerators
(3) Tributary Jitter due to pointer adjustments

Pointer Jitter - Tributary Jitter due to pointer adjustments

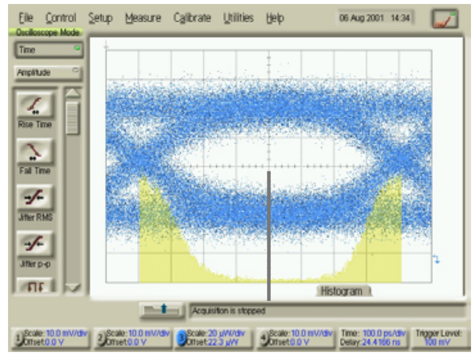
De-mapping Jitter - Tributary Jitter due to demapping process

**If timing sources S1 and S2 are precisely the same frequency,
no pointer activity will occur.**

If S1 and S2 are offset then pointer activity will occur at points 'P'

Why is jitter an important issue?

- It causes bit errors!
- Example: Several short bits in a row and eventually the sample/hold timing will try to make a decision on an edge
- From another viewpoint, the eye diagram begins to close horizontally
- If receive timing can follow the jitter, tolerance is enhanced



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•Jitter is significant only because it is one of the major potential causes for data being received in error.

•For example, if a long string of bits are on the short side, eventually a receiver will be making a decision at the edge of the bit rather than the center (if the clock rate is held constant).

•This will result in errored bits.

•Another perspective is to view the eye diagram.

•As the jitter increases, eventually the eye will close horizontally.

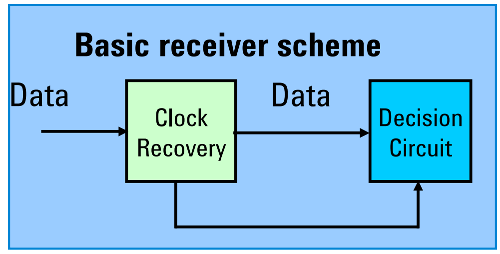
•In the waveform display, histograms have been constructed (with the horizontal slice near the crossing point) to indicate the probability of edges existing at or near the sampling point, shown by the vertical line in the center of the eye.

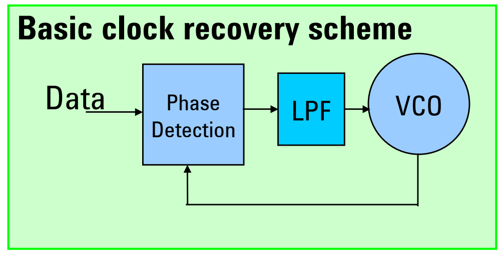
•If the clock used for setting up the sample and hold in the detection process is derived from the data, the sampling point can then follow the jitter and allow the system to tolerate jitter.

•As was the case for triggering an oscilloscope with a derived clock, the clock recovery process is limited by the loop bandwidth of the clock recovery circuitry.

Receiver timing derived from the data

- Enhances jitter tolerance
- As jitter causes the effective bit period to change, clock recovery allows receiver to stay in step
- There are practical limits on how fast and large the jitter can be





Most optical communications systems derive receiver timing from the data itself.

If the clock used to time the decision circuit were completely synchronous with the data, then any data on the jitter could be fully compensated for.

It would seem that a receiver with an infinite clock recovery loop bandwidth would be desirable.

However, from a practical design point, the error signal is low-pass-filtered (from a phase detector or virtually any other scheme that produces an error signal to drive a VCO).

Thus the bandwidth of the clock recovery scheme is limited.

Jitter that is faster than the response time cannot be tracked and will potentially lead to bit errors.

Agenda

- A review of jitter fundamentals
  - What it is and how it is generated
  - The effect of jitter on communications systems
- SONET/SDH and Ethernet timing architectures
- Characterizing jitter performance using the SONET/SDH approach
  - on transmitters
  - on receivers
- Characterizing jitter performance the Ethernet approach
  - on transmitters
  - on receivers
- Jitter measurement solutions

So far we have reviewed the basics of jitter. Now, we will turn to an explanation of the different timing architectures.

How is jitter specified?

- How much jitter is on the signals being produced?
- How much jitter can the system tolerate while maintaining a specific bit-error-ratio?
- In the process of recovering a clock signal from the data, how fast can the jitter be and did any jitter get added

Specifications for jitter can be lumped into three main categories:

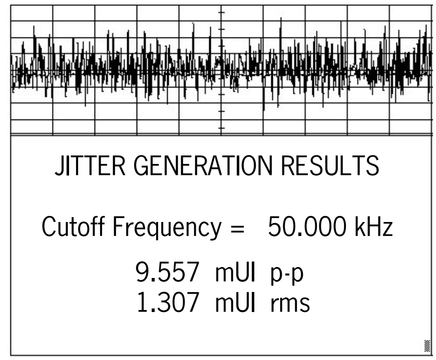
How much jitter is on the data,

How much jitter can be the system tolerate while maintaining a specific bit-error ratio,

and , in the clock recovery process, how fast can the jitter be on the signal, and was any jitter added.

Characterizing the jitter on data signals

- SONET/SDH methodology
  - Bandlimit the spectrum of the baseband jitter
    - 50 KHz to 80 MHz for OC-192/STM-64
    - to 320 MHz for OC-768/STM-256
  - Determine the peak-to-peak amplitude of the jitter
  - Specification: 0.1 UIpp



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•SONET/SDH systems are specified such that data signals cannot have more than 0.1 peak-to-peak unit intervals of jitter.

•This represents a 10% eye closure.

•It is important to note that the spectrum of the jitter is intentionally bandlimited when verifying compliance.

•Elements of the baseband jitter that are below 50 KHz and above 80 MHz for 10 g signals, and 80 KHz to 320 MHz for 40G signals (with other BW's for lower data rates) are excluded from the measurement.

•Thus measurement equipment must employ some method to reject these frequencies.

•The display shows the magnitude of the jitter versus time.

•The jitter signal has been extracted from the data.

•If the jitter is random, the waveform looks like noise.

Jitter characterization of receivers

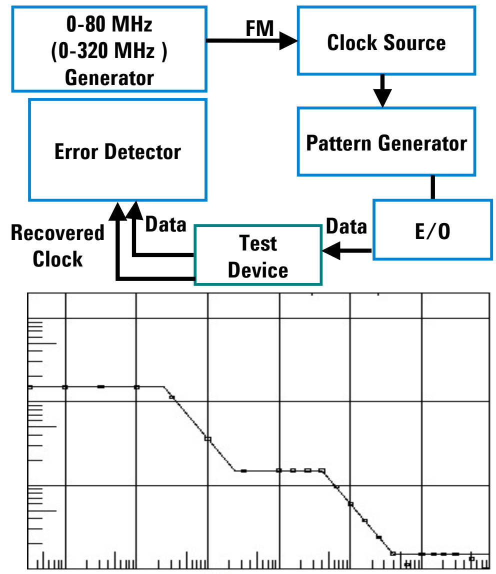
- How much jitter can be on the data signals while still maintaining a given BER level?
  - SONET/SDH: Jitter Tolerance
  - 10 Gigabit Ethernet (10 GbE): Stressed eye receiver test
- In the process of recovering a clock signal from the data, how fast can the jitter be and did any jitter get added?
  - SONET/SDH: Jitter Transfer
  - 10 GbEn: No direct assessment

The second aspect of jitter measurements involves characterizing how much jitter can be on a data signal and still allow a system to achieve an adequate BER. In SONET/SDH methodology this is called jitter tolerance. In 10 Gigabit Ethernet this is called the stressed eye receiver sensitivity. Both measurements essentially quantify the performance of receivers

In SONET/SDH, receiver jitter transfer is also characterized.

The receiver's jitter tolerance

- SONET/SDH methodology
  - Attenuate optical power to the onset of errors
  - Reduce attenuation 1 dB
  - Apply sinusoidal jitter to the data stream according to template
  - Monitor BER



•The process for performing a SONET jitter tolerance test is described as follows:

- •Attenuate optical power to the onset of errors
- •Reduce attenuation 1 dB
- •Apply sinusoidal jitter to the data stream according to the template
- •Monitor the Bit Error Ratio

•The applied sinusoidal jitter is indicated in the template diagram.

•Note that jitter initially begins at a large amplitude (in excess of 1 unit interval or full eye closure) and a low frequency.

•As the jitter frequency is increased the jitter is reduced in amplitude.

•BER measurements are made at several points along the jitter template.

Testing clock recovery: Jitter transfer

- **Definition of Jitter Transfer:**
  - **Ratio of the jitter on the recovered clock to the jitter on the incoming data as a function of jitter frequency**
- **Critical issues:**
  - **How fast can the jitter be with the recovered clock still tracking the data?**
  - **Does the clock recovery system add any jitter?**

Jitter transfer is defined as the ratio of the jitter on the recovered clock to the jitter on the incoming data as a function of jitter frequency.

Jitter transfer is used to map out the frequency response of the clock recovery circuit.

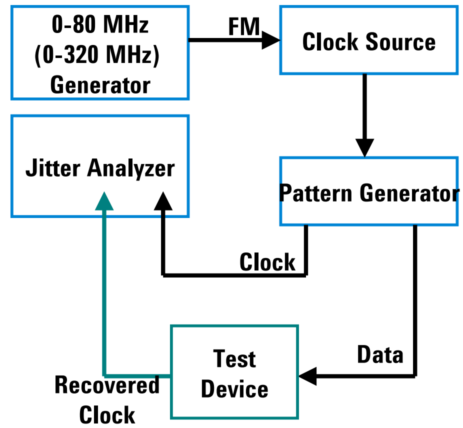
There are two critical parameters to quantify:

How fast can the jitter be with the recovered clock still tracking the data?

Does the clock recovery system add any jitter?

Assessing the speed of clock recovery:

- Sinusoidally phase modulate the data stream
- Measure the jitter on the recovered clock and compare to the jitter on the incoming data
- Sequentially increase the rate of the jitter over a specified range



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Through injecting sinusoidal jitter on the datastream, and monitoring the jitter on the recovered clock as the jitter frequency is incremented, the jitter transfer plot can be produced.

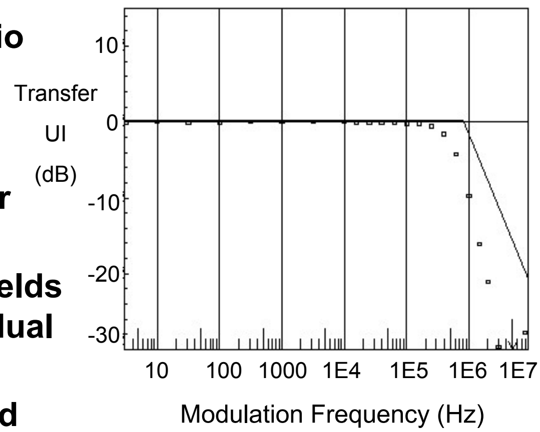
The equipment labeled “jitter analyzer’ must be capable of precisely measuring the magnitude of the sinusoidal jitter on the signal propagating from the device under test.

In some cases, the test device produces a recovered clock signal.

In other cases, the test device produces re-timed data.

Analyzing the results

- For SONET/SDH the ratio of output to input jitter should be 0 dB at low frequencies eventually rolling off at higher jitter frequencies
- Limiting the loop BW yields stability and lower residual jitter
- Only 0.1 dB gain allowed



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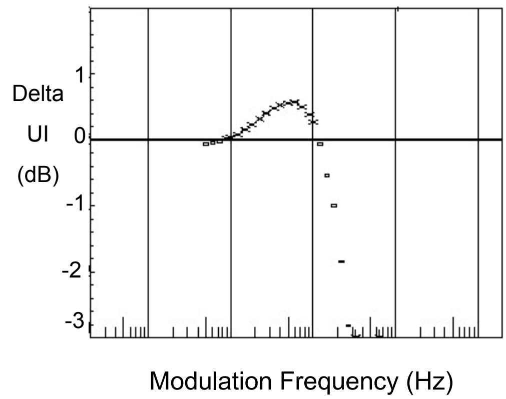
The ideal jitter transfer response would have the jitter on the recovered clock or retimed data be identical in magnitude to the jitter on the incoming data.

As the jitter gets faster and faster a point is reached where the clock recovery circuit can no longer keep up with the jitter on the data.

This filtering is intentional, as infinite bandwidth clock recovery circuits are not available. Intentionally limiting the loop bandwidth yields a higher performance system in terms of stability and the residual jitter produced on the clock signal being generated

Jitter transfer in repeater type architectures

- If the clock-recovery circuitry has any peaking in its loop filtering, the output jitter may exceed the input jitter
- If several repeaters have a similar transfer response with peaking, the overall aggregate system jitter gain can become significant



•However, designing in a low-pass filter has it's risks.

•There is the possibility that the filter response has some peaking.

•This can result in the recovered clock having larger jitter than the incoming data at the frequencies where the peaking occurs.

•In repeater type architectures timing for transmitters in SONET/SDH systems can be derived from the incoming datastream.

•If several repeaters are cascaded, each with a small amount of gain, the aggregate gain can become significant and lead to a substantial increase in jitter on the transmitted signal.

•This is the basis for the tight 0.1 dB jitter transfer specification.

•This is difficult to achieve and difficult to measure accurately.

•The above measurement example shows a clock recovery circuit with significant peaking resulting in large jitter gain.

•While this is an important parameter for SONET/SDH systems, there is no specific jitter transfer specification or measurement in 10 Gigabit Ethernet.

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- **Characterizing jitter performance the Ethernet approach**
  - **on transmitters**
  - **on receivers**
- Jitter measurement solutions

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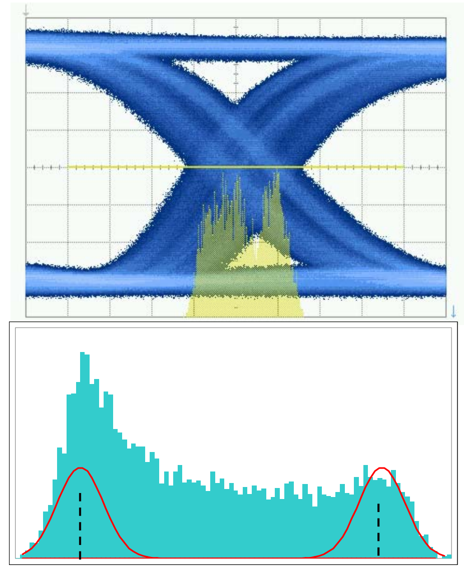
We have looked at the the SONET/SDH approach to jitter measurement methodologies.

Now, we will turn to an explanation of the Ethernet approach.

Characterizing the jitter on data signals

- 10 GbE methodology: Jitter is composed of both random and deterministic components
- Random jitter is unbounded
  - Requires a statistical analysis to be quantified
  - How far do the tails of the distribution go?



•Enterprise transmission standards have a different approach to characterizing the jitter.

•Jitter is due to both random and deterministic mechanisms.

•In that there are random elements to the jitter, the jitter is then theoretically unbounded.

•That is, if one were willing to wait long enough, the jitter magnitude could reach any value.

•In that jitter is considered to be a source of bit errors, and a 10 Gigabit Ethernet system is expected to operate at an error performance level of better than 1E-12, it would be important to characterize the probability that the jitter will consume a significant portion of the horizontal eye opening margin.

•Thus a simple “peak-to-peak” assessment of the jitter magnitude is considered inappropriate.

•The above graphs show the jitter histogram of the crossing point of a transmitter eye-diagram and a typical model of the jitter.

•The random jitter results in the tails of the histogram and should be equivalent on either side.

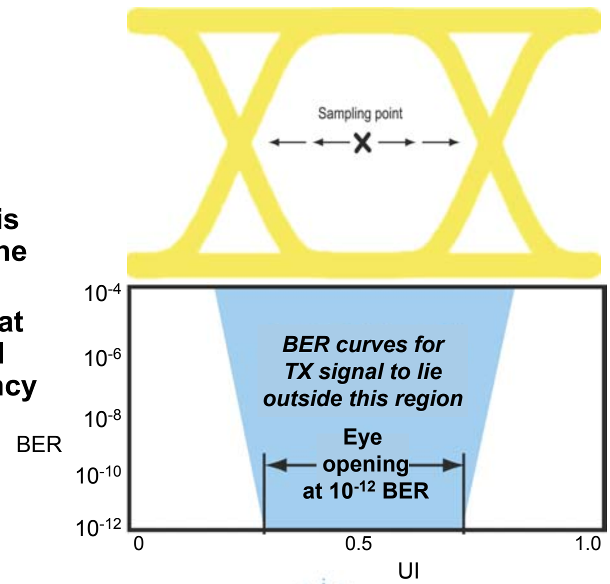
•The deterministic jitter components cause the spread between the fitted gaussian curves.

•Thus it is possible to extract both the random and deterministic components of jitter from the histogram.

•It is difficult to derive the random “tails” to a 10 E-12 precision.

Bathtub Jitter: jitter through BER measurement

- **Jitter will cause data edges to land infrequently towards the center of the eye, more frequently near the bit slot edge**
- **If the sampling point is made at the edge of the eye, errors will occur**
- **A BER measurement at a given time point will then yield the frequency at which the edges occur**
- **Plotting BER as a function of sample point time yields the bathtub curve**



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•The 10 Gigabit Ethernet approach to measuring something that is unbounded is through a bit-error-ratio measurement, specifically through a "bathtub plot".

•Consider that data jitter will result in the signal edges moving toward the center of the eye diagram.

•The extreme excursions will occur less frequently than the minor excursions.

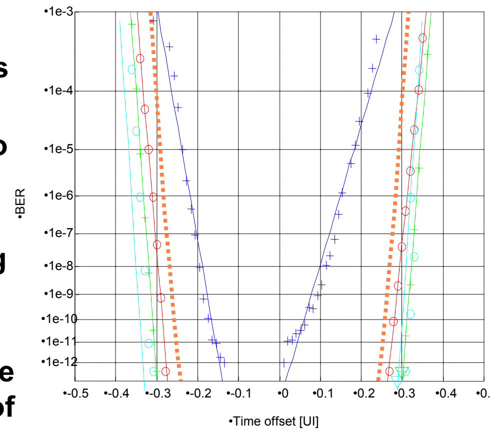
•If the transmit signal is fed to an error detector and the sampling point is optimized in both time and amplitude, the error rate should be well below 10E-12 (as close to zero as can be measured).

•As the sampling point is adjusted in time towards either of the edges of the eye, eventually a measurable BER will be reached.

•As the sampling point is continually moved into the edges of the eye, the BER will get worse and worse.

What does the bathtub curve tell us?

- A direct indication of the probability that the jitter exists at some magnitude
  - Jitter causes data edges to creep inward
  - Assume a bit error is caused by the signal being sampled at or beyond the data edge
  - BER at a given sample time manifests the probability of jitter at that time
- For 10 GbE, the jitter magnitude is specified as the eye closure at the 10E-12 BER



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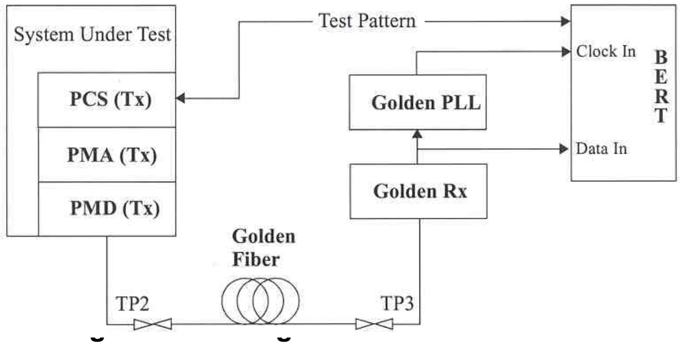
Plotting the BER as a function of the location of the sampling point time will yield the bathtub curve. The bathtub curve is then a direct indication of the probability of any magnitude of jitter up to full eye closure.

IEEE 802.3ae sets the allowable jitter magnitude at the 10E-12 BER level. Thus the “eye” must have a specified opening at this BER.

How is the bathtub curve measured?

- Specified pattern fed to transmitter
- Transmitter signal fed to golden fiber and receiver/PLL (bandwidth of 4 MHz)



- Sampling point
- Equivalent metl acceptable

Creating the bathtub curve for IEEE 802.3ae compliance goes beyond simply making a BER measurement while moving the sampling point in time.

Consider that the signal being measured is from an optical transmitter.

Error detectors are built to measure electrical signals.

Thus an optical receiver is required.

For consistency, the modulation frequency response of the receiver is specified.

The error detector needs a clock signal to time the sampling.

As discussed earlier, clock signals that have the same jitter as the signal being measured can eliminate the jitter seen on an oscilloscope.

When a clock is derived from the data and used with an error detector, the effects of jitter can also be masked.

A specific loop bandwidth clock recovery scheme is used for the bathtub jitter measurement.

The bandwidth must be less than 4 MHz.

Thus jitter on the transmitter under test that is at frequencies of 4 MHz or less is “tracked” by the error detector and does not affect the bathtub curve.

The implication here is that transmitter jitter at 4 MHz and lower is not

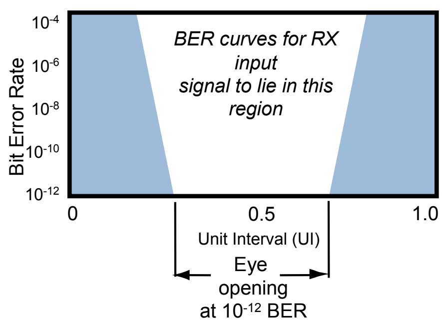
Ethernet characterization of receivers

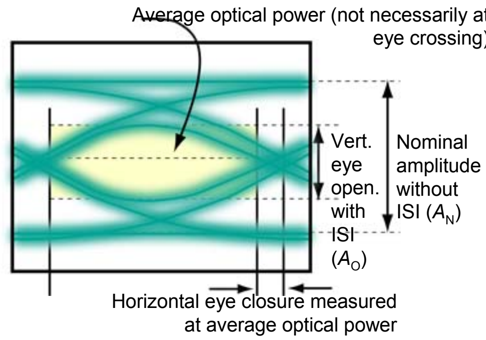
- How much jitter can be on the data signals while still maintaining a given BER level?
  - SONET/SDH: Jitter Tolerance
  - 10 GbE: Stressed eye receiver test

The second aspect of jitter measurements involves characterizing how much jitter can be on a data signal and still allow a system to achieve an adequate BER. We already explained the SONET/SDH methodology of jitter tolerance. Now we will discuss the 10 Gigabit Ethernet approach: this is called the stressed eye receiver sensitivity.

The receiver's tolerance to jitter

- 10 Gigabit Ethernet methodology: *Stressed Eye Receiver Sensitivity*
  - Apply the worst case compliant transmitter signal to the receiver
  - Verify a BER of better than 1E-12 is achieved





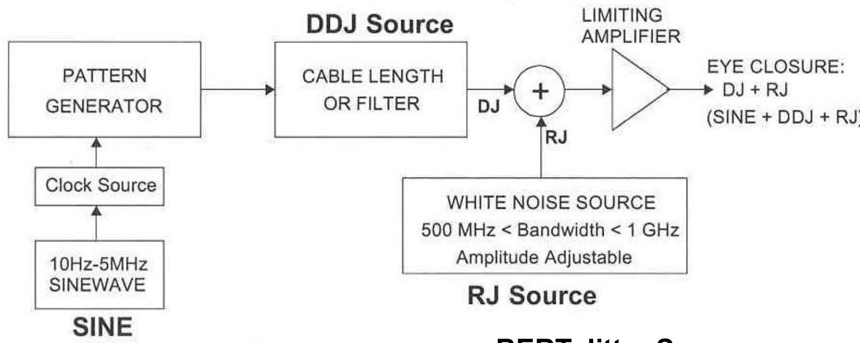
The 10 Gigabit Ethernet methodology for receiver jitter tolerance is significantly more elaborate than the SONET/SDH test, and effectively measures more than just tolerance to jitter.

The intent is to verify that a receiver is capable of operating at a BER of better than 1E-12 when presented with the worst case allowable signal.

Thus in addition to having jitter as bad as the worst case transmitter (discussed earlier in the jitter bathtub test), other impairments to the eye are also included.

The "stressed eye"

- Eye impairments include:
  - Sinusoidal jitter
  - Random jitter
  - Data dependent jitter
  - Inter-symbol interference
  - Attenuation



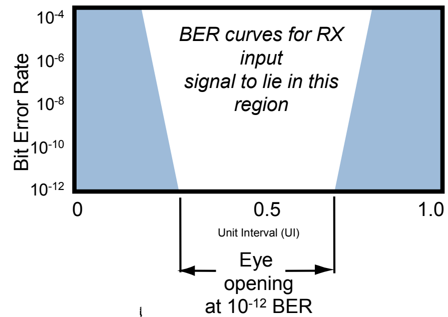
BERT Jitter Source

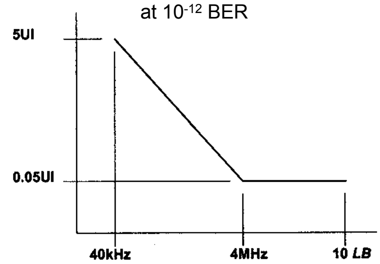
SINE: Sinusoidal Jitter Modulation
DDJ: Filter or Cable Length
RJ: White Noise Source

- The stressed eye impairments include
- The main elements of jitter are composed of random and data dependent contributions.
- Since real-world jitter is not just sinusoidal, then the receiver should be stressed with random and data dependent impairments.
- In addition, intersymbol interference and attenuation are used to degrade the signal.
- Sinusoidal jitter is used to verify operation of the receiver PLL.

Building the stressed eye

- Random and data-dependent jitter
  - The worst case jitter from a compliant transmitter
- Sinusoidal jitter:
  - Large at low frequencies, small at high frequencies





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As mentioned, the “real-world” jitter is composed of what the worst case expected jitter would be from a compliant transmitter.

Thus the template for the jitter presented to the receiver is the complement of the template for allowable transmitter jitter.

The test system must exceed the maximum allowable transmitter jitter.

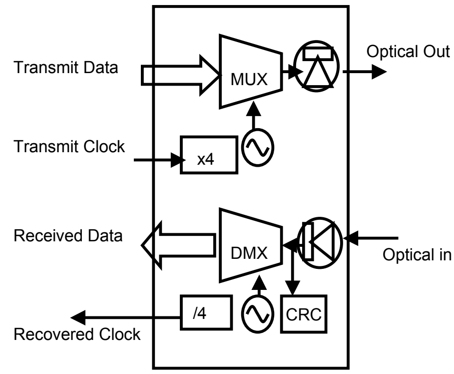
The random and deterministic jitter levels are given, but no specific methodology is given on what is used to generate these signals.

Some have created random jitter through noise injection and data-dependent jitter through specific lengths of coaxial cable preceding the test system transmitter.

Similar to SONET/SDH, sinusoidal jitter is injected according to a template that begins at large levels and low frequencies and to low levels and high frequencies.

Does clock recovery bandwidth matter?

- Not as important for 10 GbE
  - Transmitter timing not derived form the receive signal
  - Does not propagate and build
  - Response “implied” through other specifications



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In 10 Gigabit Ethernet, transmitter timing is not derived from incoming data streams.

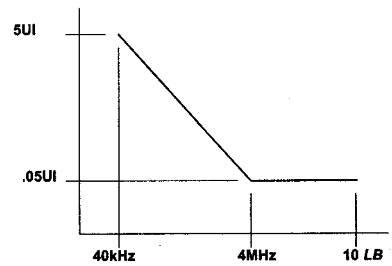
Thus jitter does not propagate from node to node, and does not have the opportunity to grow if receiver clock recovery has peaking in its transfer function.

Thus the clock recovery bandwidth is not directly quantified through a jitter transfer measurement.

However, there are elements in other tests that may result in compliance failures if the receiver has an inadequate jitter transfer function

No explicit jitter transfer requirement ….but:

- Transmitter jitter tested with “4 MHz golden PLL”
- Stressed eye includes sinusoidal jitter
- Stressed eye DJ bandlimited to 4 MHz



Stressed eye sinusoidal template

The general performance of the PLL is “exercised” through the sinusoidal jitter element of the stressed eye receiver test signal.

Significant low frequency sinusoidal jitter is injected onto the signal.

If the receiver jitter transfer corner frequency is too low, it will not be able to track the jitter and bit errors are likely to occur.

An extremely wide transfer function is difficult to produce, and is susceptible to producing a large amount of jitter on it’s own, also reducing the overall tolerance to jitter.

Agilent jitter test solutions

- Transmitter jitter
  - Bathtub curves:
    - Agilent 71612 12.5 Gbit/s error performance analyzer
    - Agilent 86130 3.6 Gbit/s error performance analyzer
    - Agilent 81250 43 Gb/s ParBERT
    - Agilent 83434 receiver

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There are a variety of solutions available from Agilent for testing jitter.

Some solutions are ideal for SONET/SDH testing, while others are more appropriate for testing according to IEEE 802.3ae 10 Gigabit Ethernet.

Any instrument capable of performing a BER measurement can be used to create a bathtub curve, as long as the sampling point can be adjusted in time.

There are three such instruments from Agilent:

the 71612C 12.5 Gb/s

The 86130 3.6 Gb/s error performance analyzers

And the 43 Gb/s ParBERT

For 10 GbEn transmitter test, the BERT should be clocked with a trigger derived from the data with a loop bandwidth of 4 MHz or less.

The Agilent 83434 lightwave receiver can convert the transmitter signal into the electrical domain and has a 4 MHz loop bandwidth to provide the appropriate clock signal to the BERT.

Agilent jitter test solutions

- **Transmitter jitter:**
  - **SONET/SDH jitter generation**
  - **SONET/SDH jitter transfer**
    - **Agilent 71501D Jitter Analysis System**
    - **Agilent JS-1000 Jitter Analysis System**
  - **Frequency agile systems, to 12.5 Gbit/s**
  - **OmniBER: SONET/SDH rates**

•For SONET/SDH characterization of transmitter jitter, an error detector is not required.

•Rather the jitter is measured directly by some form of a jitter receiver.

•Two jitter analysis systems are available from Agilent including the 71501D and JS-1000.

•The 71501D is based upon a high-speed sampling system that digitizes the waveform.

•Signal processing algorithms are then used to extract the jitter from the test signal.

•The JS-1000 system is based upon a phase-noise system that characterizes the deviation of a signal from its ideal frequency.

•The OmniBER is a dedicated compliance test system for SONET/SDH systems that has jitter detectors designed for specific SONET/SDH line rates.

Agilent jitter analysis systems

- SONET/SDH jitter tolerance:
  - Couple the Agilent 71612, or 86130 BERTs with the JS-1000 or 71501D jitter analysis systems to create a stimulus-response test set
  - OmniBER

SONET SDH jitter tolerance test requires a source of sinusoidal jitter and a method to assess bit-error-ratio.

Thus combining the previously mentioned jitter analysis systems (which produce the jitter stimulus) and an error analysis system allows the testing of BER in the presence of jitter.

The OmniBER is self-contained.

Agilent jitter analysis systems

- Ethernet “stressed eye receiver sensitivity”:
  - Stimulus: 71612C, 81250, or 86130 pattern generators
    - 71501C or JS-1000 to produce sinusoidal jitter
    - Random and data dependent jitter generators
  - Response: 71612C, 81250, 86130 error analysis

A pattern generator is required for 10 GbEn receiver test.

The data stream must also be jittered sinusoidally (71501D or E5500) as well as with Random and data dependent jitter.

The receiver response is measured with an error detector.

Agilent jitter analysis systems

- Jitter transfer:
  - 71501D (with pattern generator)
  - JS-1000 (with pattern generator)
  - OmniBER

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Jitter transfer requires sinusoidal jitter and a jitter receiver.

The jitter measurement capability must be very precise to assess jitter transfer capability within the tight 0.1 dB SONET/SDH specifications.

A pattern generator capable of sinusoidal modulation (similar to jitter tolerance testing) is required in addition to the direct jitter measurement capability.

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Agilent jitter solutions

- Wide-bandwidth oscilloscopes: “DCA’s”
  - Direct measurement of jitter in the time-domain
  - Jitter histograms
  - Residual jitter reduced to less than 200 fs rms

Digital Communications Analyzers are wide-bandwidth oscilloscopes with built-in communications analysis.

Eye diagrams and pulse trains can be analyzed for timing stability.

Recent hardware breakthroughs have provided almost an order of magnitude improvement in the residual jitter of the instrument itself.

This allows the true jitter performance of test devices to be easily seen.

(Previous instrument performance could mask the capability of high-performance, low jitter components).

DCA’s do not provide any direct assessment of the rate of jitter signals, but can be used to determine the magnitude and nature of the jitter present on a signal (clock or data).

Conclusions

- Whether it's SONET/SDH or Ethernet, jitter is a very important issue at the high Gbit/s rates
- Methodologies are similar in intent, but have significant differences in methodologies for verification
- Is one methodology better than the other?
- There is a nice overlap in the test equipment used to perform the tests

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•Jitter is one of the more difficult issues for equipment and component manufacturers and designers to deal with.

•We have examined how jitter is defined, the causes of jitter, and how it is measured.

•From a broad viewpoint, both SONET/SDH and enterprise methodologies such as 10 GbE, Fibrechannel or infiniband are trying to solve similar problems.

•However, the methodologies and reasons for verification have some distinct differences.

•It is difficult to determine if one methodology is better than another.

•The bottom line is whether functioning communication systems can be produced from both approaches.

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